Please add the following new claim:

64 (New). A method according to claim 29 further comprising:

forming a protective insulation film comprising an inorganic insulating material over said n-channel thin film transistor of said driving circuit, said pixel thin film transistor and said p-channel thin film transistor;

forming an inter-layer insulation film comprising an organic insulating material in contact with said protective insulation film; and

forming over said inter-layer insulating film a pixel electrode having a light reflecting surface and connected to said pixel thin film transistor.

## REMARKS

Applicants will address each of the Examiner's rejections in the order in which they appear in the Final Rejection.

Claim Rejections - 35 USC §103

Claims 29, 31, 33, 53-57 and 59-63

The Examiner rejects Claims 29, 31, 33, 53-57 and 59-63 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. and further in view of Yen. This rejection is respectfully traversed.

In order to advance the prosecution of this application, independent Claim 29 has been amended herein. In general, the present invention as claimed is directed to a method which is outlined below:[1]

1 In order to advance the prosecution of this application, clams 31 and 53 have been cancelled.

Low concentration n-type impurity regions are formed in first, second, and third semiconductor islands. Photoresists are then formed so that the photoresists partially overlap with each of the low concentration n-type impurity regions, respectively. Subsequently, high concentration n-type impurity regions are formed in the first, second, and third semiconductor islands using the photoresists as masks. Under the photoresist masks, the low concentration n-type impurity regions remain as they are. Then, the low concentration n-type impurity region and the high concentration n-type impurity region formed in the second semiconductor island are changed into a p-type impurity region. The second semiconductor island is formed in a p-channel thin film transistor of a driving circuit. The first semiconductor island is formed in an n-channel thin film transistor of the driving circuit. The third semiconductor island is formed in a pixel thin film transistor.

In Ohtani, impurities are implanted in a self-aligned manner. See e.g. col. 10, lns. 65-67. This is contrary to the method claimed in independent Claim 29 wherein photoresists are used when introducing an impurity.

In Fukuda, P Ion and B Ion are doped into a semiconductor of a p-channel thin film transistor without using a photoresist partially overlapping with a low concentration n-type impurity region of the p-channel thin film transistor. In contrast, in the method claimed in independent Claim 29, an impurity imparting n-type is introduced into a low concentration n-type impurity region using a photoresist mask partially overlapping with a low concentration n-type impurity region.

Yen does not suggest forming a pixel thin film transistor and a driving thin film transistor therefor over a same substrate. In contrast, in the method claimed in independent Claim 29, low concentration n-type impurity regions are formed in semiconductor islands of an n-channel thin film transistor, a p-channel transistor of a driving circuit, and a pixel thin film transistor. Further, in the

method claimed in independent Claim 29, high concentration n-type impurity regions are formed in the semiconductor islands of the n-channel thin film transistor, the p-channel transistor of the driving circuit, and the pixel thin film transistor. Furthermore, the semiconductor islands of the n-channel thin film transistor, the p-channel thin film transistor of the driving circuit, and the pixel thin film transistor are formed over a substrate in the method of independent Claim 29.

Therefore, since the method of independent Claim 29, and those claims dependent thereon, is not disclosed or suggested by the cited references, these claims are patentable thereover. Accordingly, it is requested that this rejection now be withdrawn.

Rejection of Dependent Claims 30, 32 and 58

The Examiner also has the following further rejections of the dependent claims: (i) Claim 30 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. and further in view of Yen and further in view of Zhang et al; (ii) Claim 32 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. and further in view of Yen and further in view of Yamamoto et al.; and (iii) Claim 58 under 35 U.S.C. § 103 as being unpatentable over Ohtani, in view of Fukuda et al, and further in view of Yen and in further view of Saitoj et al. Each of these rejections are respectfully traversed as each of these dependent claims are patentable over the cited references for at least the reasons discussed above for independent Claim 29.[2] Accordingly, it is respectfully requested that these rejections now be withdrawn.

Therefore, for at least the reasons discussed above, it is respectfully submitted that all of the rejections under §103 have been overcome.

2 In order to advance the prosecution of this application, Claim 32 has been cancelled.

New Claims

Applicants are also adding new dependent Claim 64 herewith. It is believed that this claim should be allowable over the art for at least the reasons discussed above. It is not believed that a fee is due for this claim. If a fee should be due, please charge our deposit account 50/1039.

Conclusion

For the above stated reasons, the present application is now in a condition for allowance and should be allowed.

If any further fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: July 7, 2003

Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street; Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Marked-up copy of the claims as amended:

**IN THE CLAIMS**:

Please amend the claims as follows:

29 (Twice Amended). A method of fabricating a semiconductor device [having, on the same substrate, a pixel TFT disposed in a pixel unit and a driving circuit including a p channel type TFT and an n channel type TFT and disposed round said pixel unit, said method] comprising:

[forming an underlying film over said substrate;

forming a plurality of semiconductor islands over said underlying film;

forming n type impurity regions having a first concentration, for forming LDD regions of said n channel type TFT of said driving circuit and said pixel TFT in selected regions of said semiconductor islands;

forming n type impurity regions having a second concentration, for forming source regions or drain regions outside said LDD regions by introducing an n-type impurity thereinto while covering at least said LDD regions of said n channel type TFT of said driving circuit and said pixel TFT with resist masks, respectively;

forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT of said driving circuit in a selected region of said semiconductor islands;

forming a protective insulation film comprising an inorganic insulating material over said n channel type TFT of said driving circuit, said pixel TFT and said p channel type TFT;

forming an inter-layer insulation film comprising an organic insulating material in close contact with said protective insulation film; and

forming over said inter-layer insulating film a pixel electrode having a light reflecting surface and connected to said pixel TFT]

forming a first semiconductor island and a second semiconductor island and a third semiconductor island over a substrate;

forming a first low concentration n-type impurity region and a second low concentration n-type impurity region and a third low concentration n-type impurity region respectively in said first semiconductor island and said second semiconductor island and said third semiconductor island by introducing a first impurity imparting n-type into said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region;

forming a first photoresist and a second photoresist and a third photresist respectively over said first semiconductor island and said second semiconductor island and said third semiconductor island so that said first photoresist partially overlaps with said first low concentration n-type impurity region and said second photoresist partially overlaps with said second low concentration n-type impurity region and said third photoresist partially overlaps with said third low concentration n-type impurity region;

forming a first high concentration n-type impurity region and a second high concentration n-type impurity region and a third high concentration n-type impurity region respectively in said first semiconductor island and said second semiconductor island and said third semiconductor island by introducing a second impurity imparting n-type into a first part of each of said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region using said first photoresist and said second photoresist and said

third photoresist as masks to leave behind second parts provided under said masks in said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region as they are; and

introducing impurities imparting p-type into said second low concentration n-type impurity region and said second high concentration n-type impurity region to change said second low concentration n-type impurity region and said second high concentration n-type impurity region to a p-type impurity region,

wherein concentration of said second impurity is higher than concentration of said first impurity,

wherein said first semiconductor island is formed in an n-channel thin film transistor of a driving circuit,

wherein said second semiconductor island is formed in a p-channel thin film transistor of said driving circuit, and

wherein said third semiconductor island is formed in a pixel thin film transistor.

30 (Twice Amended). A method according to claim [29] 64, wherein, [as for] said p-type impurity region is formed in said p channel [type TFT] thin film transistor of said driving circuit [, the step of forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT is conducted] in a selected region of said second semiconductor island[s] after said step of forming said protective insulation film comprising an inorganic insulating material, over [the] a gate electrode of said p channel [type TFT] thin film transistor, and an offset region is formed between [the] a channel formation region of said p channel

[type TFT] thin film transistor and said p type impurity region [having the third concentration, for forming the source region or the drain region].

Cancel Claims 32, 33 and 53.

54 (Amended). A method according to claim [29] 64 wherein said protective insulation film comprises a material selected from the group consisting of silicon oxide, silicon oxide nitride and silicon nitride.

55 (Amended). A method according to claim [29] 64 wherein said protective insulation film has a thickness of 100 to 200 nm.

56 (Amended). A method according to claim [29] 64 wherein said inter-layer insulation film has a mean thickness of 1.0 to 2.0 μm.

57 (Amended). A method according to claim [29] 64 wherein said inter-layer insulation film comprises a material selected from the group consisting of polyimide, acryl, polyamide, polyimidamide and benzocyclobutene.

58 (Amended). A method according to claim [29] 64 wherein said pixel electrode comprises a Ti film and an Al film.

59 (Amended). A method according to claim 29 wherein said p channel [type TFT] thin film transistor has a single drain structure.

60 (Amended). A method according to claim 29 wherein said first low concentration n-type impurity region of said first semiconductor island formed in [LDD regions of] said n channel [type TFT] thin film transistor of said driving circuit have a length of 1.0 to 4.0 μm.

61 (Amended). A method according to claim 29 wherein [said LDD regions of said n channel type TFT of] said third low concentration n-type impurity region of said third semiconductor island formed in said pixel [TFT] thin film transistor have a length of 0.5 to 4.0 μm.

62 (Amended). A method according to claim 29 wherein said first and second and third semiconductor islands have a thickness of 25 to 80 μm.

Please add the following new claim:

64 (New). A method according to claim 29 further comprising:

forming a protective insulation film comprising an inorganic insulating material over said n-channel thin film transistor of said driving circuit, said pixel thin film transistor and said p-channel thin film transistor;

forming an inter-layer insulation film comprising an organic insulating material in contact with said protective insulation film; and

forming over said inter-layer insulating film a pixel electrode having a light reflecting surface and connected to said pixel thin film transistor.